Remarks:

Reconsideration of the application is respectfully requested.

Claims 1 - 25 are presently pending in the application. Claims 1 has been amended. In item 5 of the above-identified Office Action, it was indicated that the "capable of" terminology allegedly does not positively claim the limitation and was, therefore, given no weight. Applicants have amended claim 1 to better clarify the language of that claim. The above-noted changes to the claims are provided solely for clarification or cosmetic reasons. The changes are neither provided for overcoming the prior art nor do they narrow the scope of the claim for any reason related to the statutory requirements for a patent.

In item 3 of the Office Action, claims 1 - 5, 16 - 23 and 25 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U. S. Patent No. 5,870,619 to Wilkinson et al ("**WILKINSON**"). Applicant notes that **WILKINSON** published on February 9, 1999, and that the present case claims priority from a German Application filed on September 23, 1998. As such, the proper basis for rejecting the Applicants' claims under 35 U.S.C. § 102, in view of **WILKINSON**, would be to allege anticipation under 35 U.S.C. § 102(e). As such, Applicants will treat the rejection of item 3 as a 35 U.S.C. § 102(e) rejection.

In item 15 of the Office Action, claims 6 - 15 and 24 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over **WILKINSON**.

Applicants respectfully traverse the above rejections.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 recites a configurable hardware block, comprising:

> "a universal configurable unit being selectively configured to read data stored in a memory unit, to process the data in at least one of arithmetic and logical processing units, and to write data representing a result of the processing to the memory unit, **said universal configurable unit having an asynchronous combinational circuit to asynchronously link components of said universal configurable unit**, and said universal configurable unit being capable of interacting autonomously with external hardware." [emphasis added by Applicants]

As noted above and in the responses to the two previous substantive Office Actions, Applicants' claims all require, among other limitations, **an asynchronous combinational circuit to asynchronously link components of the universal configurable unit.** This is supported in paragraph [0050] of the instant application, which states:

> UCB read and write accesses to the memory unit should preferably be timed. The UCB itself is an asynchronous combinational circuit between the inputs and outputs

> of the memory unit. **The components of the UCB are linked together asynchronously.** [emphasis added by Applicants]

The **WILKINSON** reference, cited against all the claims in the present case, fails to teach or suggest, among other limitations of Applicants' claims, **an asynchronous combinational circuit to asynchronously link components of the universal configurable unit.**

More particularly, **WILKINSON** discloses an **array processor** comprising a plurality of memory elements. Col. 17 of **WILKINSON,** lines 3 - 17, discloses a "picket system" employing a processor, wherein each processor is formed from a gate array. According to col. 17 of **WILKINSON**, the processor of each picket system is scalable. Col. 7 of **WILKINSON**, lines 15 - 19 define a **picket processor system (or subsystem)** as:

> "A picket processor is a total system consisting of an array of pickets, a communication network, an I/O system, and a SIMD controller consisting of a microprocessor, a canned routine processor, and a micro-controller that runs the array."

Col. 6 of **WILKINSON**, line 58 - col. 7, line 11, defines a **"picket"**, as:

> "This is the element in an array of elements making up an array processor. It consists of: data flow (ALU REGS), memory, control, and the portion of the communication matrix associated with the element. The unit refers to a 1/nth of an array processor made up of parallel processor and memory elements with their

control and portion of the array intercommunication mechanism. A picket is a form of processor memory element or PME. Our PME chip design processor logic can implement the picket logic described in related applications or have the logic for the array of processors formed as a node. The term PICKET is similar to the commonly used array term PE for processing element, and is an element of the processing array preferably comprised of a combined processing element and local memory **for processing bit parallel bytes of information in a clock cycle**. The preferred embodiment consisting of a byte wide data flow processor, 32 k bytes or more of memory, primitive controls and ties to communications with other pickets.

The term "picket" comes from Tom Sawyer and his white fence, although it will also be understood functionally that a military picket line analogy fits quite well." [emphasis added by Applicants]

Col. 17 of **WILKINSON**, lines 18 - 21, states:

"Fig. 2 illustrates the memory processor which we call the PME or processor memory element in accordance with our preferred embodiment. **The processor has eight or more processors.** In the pictured embodiment there are eight." [emphasis added by Applicants]

Col. 7 of **WILKINSON**, lines 31 - 41 define a PME as follows:

"PME or processor memory element

PME is used for a processor memory element. We use the term PME to refer to a single processor, memory and I/O capable system element or unit that forms one of our parallel array processors. A processor memory element is a term which encompasses a picket. A processor memory element is 1/nth of a processor array which comprises a processor, its associated memory, control interface, and a portion of an array communication network mechanism. **This element can have a processor memory element with a connectivity of a regular array, as in a picket processor, or as part of a subarray, as in the multi-processor memory**

> **element node we have described.**" [emphasis added by Applicants]

It is inferred from item 4 of the Office Action that these **processor arrays** or **multi-processor memory element nodes** of **WILKINSON** were what was alleged in the Office Action to be analogous to Applicants' claimed "**universal configurable unit**". Applicants' respectfully disagree. As stated above, all of Applicants' claims recite, among other limitations:

> **"said universal configurable unit <u>having an asynchronous combinational circuit to asynchronously link components</u> of said universal configurable unit"** [emphasis added by Applicants]

First, as disclosed in col. 72 of **WILKINSON**, lines 7 - 11:

> "The Picket, or the array controller, can assign the picket to one or more of several groups. A picket can be in more that [sic] one group simultaneously. Groups can be selected for certain parts of a process in either SIMD or MIMD mode, and may be freely moved between these."

However, it is important to note that, as shown in the definition of **pickets** in **WILKINSON**, cols. 6 - 7, **<u>pickets are synchronous elements</u>** (i.e.,"is an element of the processing array preferably comprised of a combined processing element and local memory **for processing bit parallel bytes of information <u>in a clock cycle</u>"**). As such, **pickets**, the elements pointed to in the Office Action as providing the

basic reconfigurable building blocks of **WILKINSON** require synchronization.

Further, the Office Action, on page 2, cites col. 69 of **WILKINSON**, line 26 - col. 70 - line 38 and col. 72, lines 35 - 46, as allegedly disclosing that the processor arrays and/or multi-processor memory element nodes of **WILKINSON** are linked asynchronously. Applicant respectfully disagrees. Directly contrary to the alleged teaching, and contrary to Applicants' claimed invention, col. 70 of **WILKINSON** teaches that the picket processors **forming the array** are synchronized. More particularly, **WILKINSON** discloses in col. 70, lines 9 - 11 that while computing locally in the MIMD mode, a node needs no synchronization. However, like the Baxter reference of the prior Office Action, when communication between processor units is needed in the **WILKINSON** system, **synchronization is needed**. This is disclosed in col. 70 of **WILKINSON**, lines 3 - 29, which states:

> "Some of our features which are advances in the art at the time we developed the picket machine include the SIMIMD function. Our SIMIMD function provides that a picket memory is loaded with small amounts of program code which is executed which is executed by each picket. Control is retained by the controller, after which additional small amounts of code may be loaded and executed. **The processing unit in MIMD mode provides the ability to do independent things in each picket processing unit. It is now not necessary to transfer an entire program to an array processor.** An entire program would not normally be transferred to the Pickets.

> For example, a partition manage could load identical code onto every processing node in a partition. Data would be distributed across nodes. Given an array of m values and a partition of n nodes, each node would then handle m/n values. **As each node can execute the portion of its program in its MIMD mode independently, branching according to its own data values, as long as computation remains local, no synchronization or communication is needed. When data needs to be transferred among processors, for example when processors must each contribute values to a global sum, the communication networks carry the data and enforce the necessary synchronization.** For global combining operations such as sum, the controller functions to organize the controlled network to perform the reduction." [emphasis added by Applicants]

This is further clarified in col. 71 of **WILKINSON**, lines 49 - 55, which states:

> "Our controller and controlled network functions **include synchronization of processing nodes (and processing elements within a node)**, combining a value from every processing element to produce a single result, and can computer parallel prefix operations. Our picket processor provides a separate control network and data network. See U.S. Ser. No. 611,594 and other related applications." [emphasis added by Applicants]

Thus, it is believed that in **WILKINSON**, although each processor of an **array** can act asynchronously, it is believed that the processors or components within the **array** are synchronized by a controller when linking to each other. Applicants note that the terminology of **WILKINSON** is confusing, as several different levels of cooperative elements are referred to as "processor". This is best illustrated by

the sentence in col. 17 of **WILKINSON**, lines 20 - 21, stating "The **processor** has eight or more **processors**." However, it is believed that, **on the array and node level** (i.e., argued to be analogous to Applicants' claimed "universal configurable unit "), the processors of **WILKINSON** are synchronized (i.e., **not asynchronously linked**).

Note that **WILKINSON** discloses a SIMD processor mode(i.e., "a processor array architecture wherein all processors in the array are commanded from a Single Instruction stream to execute Multiple Data streams located one per processing element"; col. 7 of **WILKINSON**, lines 55 - 59) . As stated in col. 69 of **WILKINSON**, lines 39 - 43:

> "If several elements are executing a copy of the same instruction stream, and they are **synchronized such that they run more or less synchronously,** then an APAP or other such machine **could emulate our picket SIMD architecture**." [emphasis added by Applicants]

As such, it is believed that **WILKINSON** fails to teach or suggest **an asynchronous combinational circuit to asynchronously link components of the universal configurable unit**, as required by Applicants' claims.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1. Claim 1 is, therefore, believed to

be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1. As it is believed that the claims were patentable over the cited art in their original form, the claims have not been amended to overcome the references.

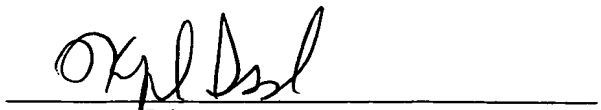
In view of the foregoing, reconsideration and allowance of claims 1 - 25 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,



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For Applicants

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